Electronic Version
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Claims

[c1] 1. A conductive memory device comprising:

a bottom electrode having a top face with a first surface area;

a top electrode located above the bottom electrode having a bottom face with a second surface area; and

a multi-resistive state element sandwiched between the bottom electrode and the top electrode and having a bottom face with a third surface area and a top face with a fourth surface area, the multi-resistive state element's bottom face being in contact with the bottom electrode's top face, and the multi-resistive state element's top face being in contact with the top electrode's bottom face;

wherein the fourth surface area is not equal to the second surface area.

[c2] 2. The conductive memory device of claim 1 further comprising:

a diffusion barrier;

wherein the bottom electrode, the top electrode and the multi-resistive state element each have sides that are adjacent to their faces, the sides being covered

by the diffusion barrier.

[c3] 3. The conductive memory device of claim 2 wherein the diffusion barrier is also an etch stop.

[c4] 4. The conductive memory device of claim 2 wherein the diffusion barrier is Si_3N_4, TiO_2 or Al_2O_3.

[c5] 5. The conductive memory device of claim 1 wherein the first surface area is larger than the third surface area.

[c6] 6. The conductive memory device of claim 1 wherein the second surface area is larger than the fourth surface area.

[c7] 7. The conductive memory device of claim 1 further comprising

a sidewall layer

wherein the bottom electrode, the top electrode and the multi-resistive state element each have sides that are adjacent to their faces, the sides being at least partially covered by the sidewall layer.

[c8] 8. The conductive memory device of claim 1 wherein the second surface area is smaller than the fourth surface area.

[c9] 9. The conductive memory device of claim 8 further comprising:

a hard mask layer having a bottom face with a surface area substantially similar to the second surface area;

wherein the top electrode has a top face that is in contact with the bottom face of the hard mask layer.

[c10] 10. The conductive memory device of claim 8 further comprising:

a spacer;

wherein the top electrode has sides adjacent to its bottom face, the spacer surrounding the sides.

[c11] 11. The resistive memory device of claim 10 wherein the spacer has a bottom face that is in contact with the top face of the multi-resistive state element such that the spacer's width makes up for the cross sectional difference between the top electrode's bottom face and the multi-resistive state element's top face, thereby ensuring complete coverage of the multi-resistive state element's top face.

[c12] 12. The conductive memory device of claim 10 wherein the spacer is a dielectric material.

[c13] 13. The conductive memory device of claim 12 wherein:

the multi-resistive state element has sides that are adjacent to its faces; and

the spacer's width is large enough to make the detrimental effect of any leakage current conduction between the top electrode and the bottom electrode near the sides of the multi-resistive state element negligible.

[c14] 14. The conductive memory device of claim 12 wherein the dielectric material is Si_3N_4, SiO_2, TiO_2, SiON or Al_2O_3.

[c15] 15. The conductive memory device of claim 10 further comprising:

a sidewall layer;

wherein the bottom electrode, the top electrode and the multi-resistive state element each have sides that are adjacent to their faces, the sides being at least partially covered by the sidewall layer.

[c16] 16. The conductive memory device of claim 1 wherein, expressed in an X-Y-Z Cartesian coordinate system:

the top and bottom faces of the bottom electrode, the top electrode and the multi-resistive state element lie essentially in the X-Y plane; and

the direction of current conduction through the conductive memory device is essentially parallel to the Z-axis.

[c17] 17. A method of making a plurality of conductive mem-

ory devices comprising:

forming a bottom electrode layer;

forming a multi-resistive state element layer;

forming a top electrode layer;

forming a hard mask layer;

patterning the hard mask layer and the top electrode layer such that the patterned top electrode and hard mask have a first cross sectional area;

forming a dielectric material layer;

etching the dielectric material to create a sidewall spacer; and

etching the multi-resistive state element layer and the bottom electrode layer using the hard mask such that the etched bottom electrode and multi-resistive state element have a second cross sectional area that is larger than the first cross sectional area.

[c18] 18. A method of making a plurality of conductive memory devices, each conductive memory device operable to be reversibly placed in multiple resistive states, the method comprising:

sputtering a bottom electrode layer;

sputtering a multi-resistive state element layer;

sputtering a top electrode layer;

depositing a hard mask layer;

photo lithographically patterning the hard mask layer

and the top electrode layer such that the patterned top electrode and hard mask have a first cross sectional area;

depositing a dielectric material;

etching the dielectric anisotropically to create a sidewall spacer at the edges of the top electrode; and

etching the multi-resistive state element layer and the bottom electrode layer using the hard mask such that the etched bottom electrode and multi-resistive state element have a second cross sectional area that is larger than the first cross sectional area.

[c19] 19. The method of making a plurality of conductive memory devices of claim 18 wherein the multi-resistive state element layer and the top electrode layer have an interface that is modified.

[c20] 20. The method of making a plurality of conductive memory devices of claim 19 wherein modification of the interface is performed by either ion implantation, in situ argon plasma treatment, in situ oxygen plasma treatment, in situ annealing in argon or in situ annealing in oxygen.

[c21] 21. The method of making a plurality of conductive memory devices of claim 18 further comprising:

wet etching the multi-resistive state element layer

wherein the wet etching is performed after the etching of the multi-resistive state element layer, the etching of the multi-resistive state element layer forming multi-resistive state element sides; and wherein the wet etching of the multi-resistive state element removes a thickness of 50 -150 Å, thereby forming an undercut from the multi-resistive state element sides.

[c22] 22. The method of making a plurality of conductive memory devices of claim 18 wherein at least one etching is performed via high temperature reactive ion etching.